The Applicant requests under MPEP §806.05(c) that the Examiner provide reasonable examples that recite material differences. The Applicant disagrees with the Examiner's blanket assertion that "any other apparatus which supports fix point and floating point operations" can perform the process of claim 9. Claim 9 refers to using an array processor for frame rendering and DSP applications and lists certain limitations in performing these operations. Thus as required by MPEP §806.05(c), the Applicant requests an example of a materially different apparatus .

Although the Applicant traverses the restriction requirement, Applicant makes a provisional election of Group I, claims 1-8.

Rejections under 35 U.S.C. §103(a)

Claims 1-8 were rejected under 35 U.S.C. §103(a) as being unpatentable by Ngai. Claim 8 has been canceled.

Ngai is a pipelined paralleled vector processor that performs arithmetic operations on vectors in vector registers by performing arithmetic operations on subsets of the vectors (col. 1, lines 61-66, col. 3, lines 36-55). The vectors are stored in main memory (52) and transferred to one or more vector registers (col. 4, lines 56-59, col. 5, lines 25-28).

Claim 1 recites an integrated circuit for image frame rendering and DSP applications, the integrated circuit during operation operating with memory. The integrated circuit includes: an interface circuit configured to control access to said memory, the interface circuit coupled to said memory; an embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom; and an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom. The array processor includes , a shared operand unit for providing a shared operand.

Claim 1 is distinguishable from Ngai, in that Ngai does not have or suggest a shared operand unit. The Examiner is incorrect in suggesting main memory 52 is the shared operand circuit. There is no suggestion or teaching in Ngai that main memory 52 is other than a general storage unit. In addition under MPEP §2143, to establish a prima facie case of obviousness, the prior art reference must teach or suggest all claim limitations. The Examiner does not state what in the prior art maps to "said memory" in claim 1. Assuming, for the sake

of argument, that main memory 52 maps to "said memory" of claim 1, there is no teaching or suggestion by Ngai of a shared operand circuit. Thus no case of prima facie obviousness has been established. For at least these reasons claim 1 should be allowable.

Claims 2-7 being dependent on claim 1 should be allowable for at least the same reasons claim 1 is allowable.

In addition concerning claim 2 , the applicant traverses the Examiner's assertion that use of simplified IEEE floating point notation in image frame rendering and DSP applications is obvious, and under MPEP §2144.03, the applicant requests a reference.

Claims 1-8 were rejected under 35 U.S.C. §103(a) as being unpatentable by Wang. Claim 8 has been canceled.

Wang is a vector co-processing system for robotic control. A host processor 18, such as a Sun workstation, provides the user interface and communicates with the vector co-processor 20 through VME bus 19 (col. 7, lines 44-49, Fig. 2). Fig. 3 shows a diagram of the internals of processor 20 and shows the VME bus and private bus 24 between the processor 20 and other parts of the robotic system (col. 8, lines 42-47).

Wang is distinguishable from claim 1, in that Wang does not teach nor suggest an interface circuit configured to control access to said memory, the interface circuit coupled to said memory; nor an embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom. The Examiner's assertion that the buses are the interface circuit is incorrect. The VME bus 19 and private bus 24 are 32-bit buses and not an interface circuit configured to control access to a memory. In addition the host processor 18 is a host workstation in Wang and not an embedded processor configured to control the integrated circuit. Thus Wang does not teach nor suggest these two claim 1 limitations. Hence no case of prima facie obviousness has been established. For at least these reasons claim 1 should be allowable.

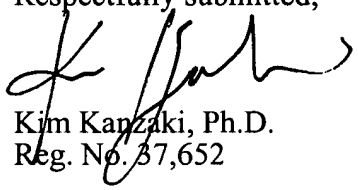
Claims 2-7 being dependent on claim 1 should be allowable for at least the same reasons claim 1 is allowable.

In addition the Examiner's assertion that in claims 3 and 5 , the wire bundle would obviously exceed 256 wires is incorrect. In Wang the preferred bus size is 32-bits (col. 8, lines 46-47). Thus claims 3 and 5 should be allowable over Wang.

## CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 650-326-2400.

Respectfully submitted,



Kim Kanzaki, Ph.D.
Reg. No. 37,652

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (650) 326-2400
Fax: (415) 576-0300
KK:amc
PA 3115330 v1